

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF4024B**

## **MSI**

## **7-stage binary counter**

Product specification  
File under Integrated Circuits, IC04

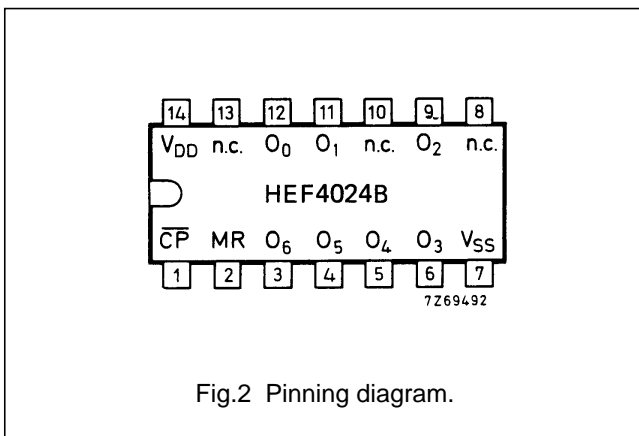
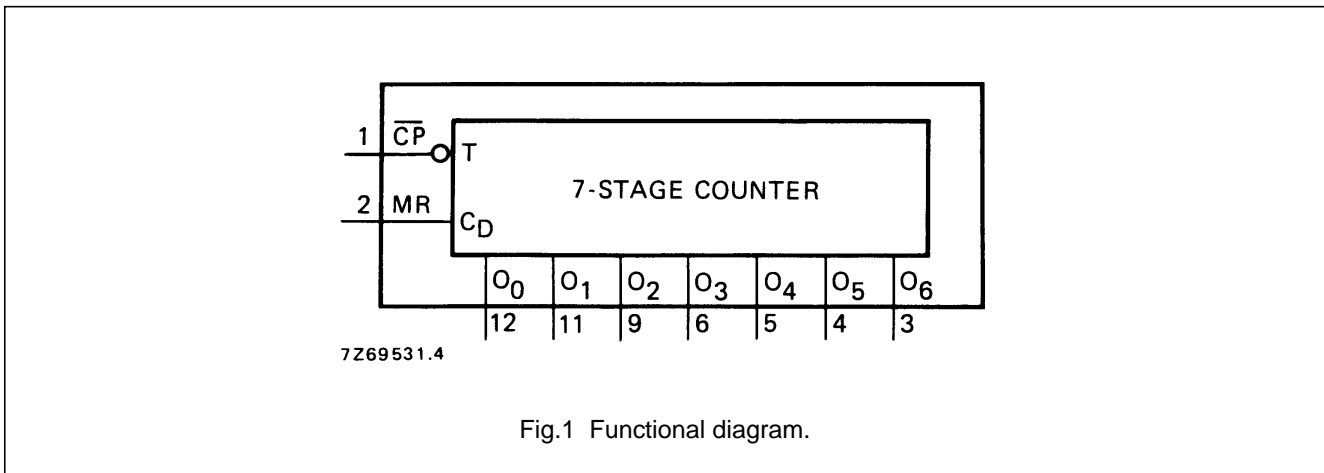
January 1995

# 7-stage binary counter

**HEF4024B**  
**MSI**

## DESCRIPTION

The HEF4024B is a 7-stage binary ripple counter with a clock input ( $\overline{CP}$ ), and overriding asynchronous master reset input (MR) and seven fully buffered parallel outputs ( $O_0$  to  $O_6$ ). The counter advances on the HIGH to LOW transition of  $\overline{CP}$ . A HIGH on MR clears all counter stages and forces all outputs LOW, independent of  $\overline{CP}$ . Each counter stage is a static toggle flip-flop.



## PINNING

- $\overline{CP}$  clock input (HIGH to LOW triggered)
- MR master reset input
- $O_0$  to  $O_6$  buffered parallel outputs

## APPLICATION INFORMATION

Some examples of applications for the HEF4024B are:

- Frequency dividers
- Time delay circuits

## FAMILY DATA, $I_{DD}$ LIMITS category MSI

See Family Specifications

- HEF4024BP(N): 14-lead DIL; plastic (SOT27-1)
- HEF4024BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
- HEF4024BT(D): 14-lead SO; plastic (SOT108-1)
- ( ): Package Designator North America

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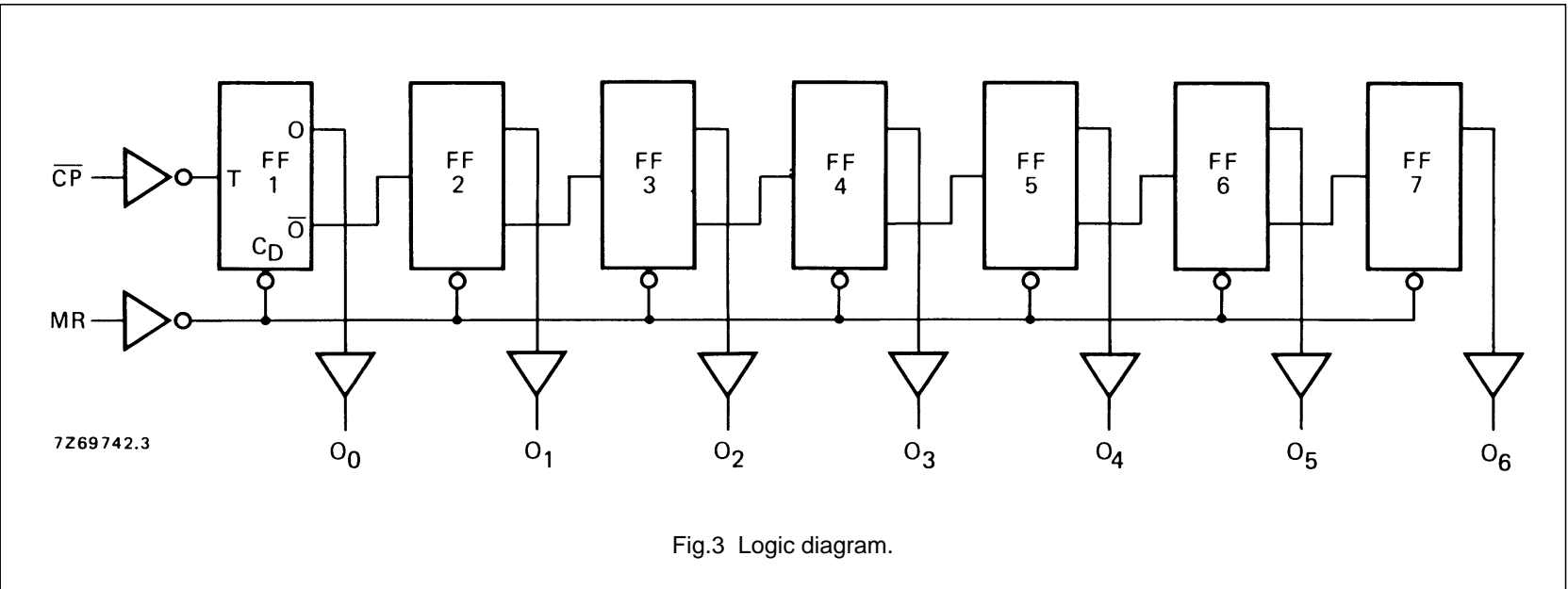


Fig.3 Logic diagram.

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MSI**AC CHARACTERISTICS** $V_{SS} = 0$  V;  $T_{amb} = 25$  °C;  $C_L = 50$  pF; input transition times  $\leq 20$  ns; see also waveforms Fig.4

	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA		
Propagation delays	$\overline{CP} \rightarrow O_0$ HIGH to LOW	$t_{PHL}$		100	200	ns	73 ns + (0,55 ns/pF) $C_L$	
			5	40	75	ns	29 ns + (0,23 ns/pF) $C_L$	
			10	25	50	ns	17 ns + (0,16 ns/pF) $C_L$	
	LOW to HIGH	$t_{PLH}$		105	210	ns	78 ns + (0,55 ns/pF) $C_L$	
			5	45	85	ns	34 ns + (0,23 ns/pF) $C_L$	
			10	30	60	ns	22 ns + (0,16 ns/pF) $C_L$	
	$O_n \rightarrow O_{n+1}$ HIGH to LOW	$t_{PHL}$		60	120	ns	33 ns + (0,55 ns/pF) $C_L$	
			5	25	50	ns	14 ns + (0,23 ns/pF) $C_L$	
			10	20	40	ns	12 ns + (0,16 ns/pF) $C_L$	
		LOW to HIGH	$t_{PLH}$		50	100	ns	23 ns + (0,55 ns/pF) $C_L$
				5	20	40	ns	9 ns + (0,23 ns/pF) $C_L$
				10	15	30	ns	7 ns + (0,16 ns/pF) $C_L$
MR $\rightarrow O_n$ HIGH to LOW	$t_{PHL}$		120	240	ns	93 ns + (0,55 ns/pF) $C_L$		
		5	45	90	ns	34 ns + (0,23 ns/pF) $C_L$		
		10	30	60	ns	22 ns + (0,16 ns/pF) $C_L$		
Output transition times	HIGH to LOW	$t_{THL}$		60	120	ns	10 ns + (1,0 ns/pF) $C_L$	
			5	30	60	ns	9 ns + (0,42 ns/pF) $C_L$	
			10	20	40	ns	6 ns + (0,28 ns/pF) $C_L$	
	LOW to HIGH	$t_{TLH}$		60	120	ns	10 ns + (1,0 ns/pF) $C_L$	
			5	30	60	ns	9 ns + (0,42 ns/pF) $C_L$	
			10	20	40	ns	6 ns + (0,28 ns/pF) $C_L$	
Minimum clock pulse width; HIGH	$t_{WCPH}$		60	30	ns			
		5	30	15	ns			
		10	20	10	ns			
Minimum MR pulse width; HIGH	$t_{WMRH}$		80	40	ns			
		5	35	20	ns			
		10	25	15	ns			
Recovery time for MR	$t_{RMR}$		20	10	ns			
		5	15	5	ns			
		10	15	5	ns			
Maximum clock pulse frequency	$f_{max}$		5	10	MHz			
		5	13	25	MHz			
		10	18	35	MHz			

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	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu$ W)	
Dynamic power dissipation per package (P)	5	$500 f_i + \sum (f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load cap. (pF) $\sum (f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)
	10	$2100 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$5200 f_i + \sum (f_o C_L) \times V_{DD}^2$	

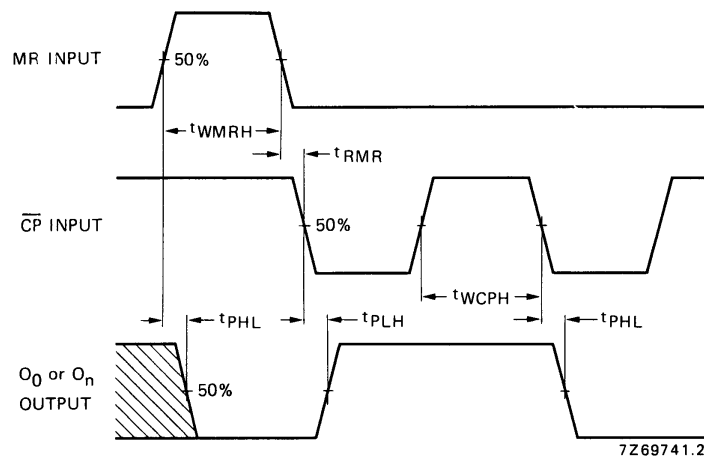


Fig.4 Waveforms showing propagation delays for MR to O<sub>n</sub> and CP to O<sub>0</sub>, minimum MR and CP pulse widths and recovery time for MR.